a feedback path to provide an output of said pulse generator to said activation circuit, said feedback path including an inverter to create a high signal in response to a low signal on said feedback path.

Please cancel claims 14 and 15.

Please amend claim 16 as follows:

16 (Amended). The integrated circuit of claim 11 including a pair of transistors that must both conduct in order to generate said pulses.

Please add the following new claims 31 *et seq.*

31 (New). A method comprising:

developing a pulse indicating that a power supply voltage is not in a first state using a first circuit; and

latching the first circuit in response to the power supply voltage being in the first state using a second circuit.

32 (New). The method of claim 31 including latching the first circuit using the second circuit until the next power cycle.

33 (New). The method of claim 31 including using a logic functionality that emulates logic that is difficult to trigger.

34 (New). The method of claim 31 including detecting when a voltage is above at least two transistor threshold voltages using said second circuit to control said first circuit.

35 (New). The method of claim 31 including feeding back the output from the first circuit to the second circuit.

36 (New). The method of claim 35 including inverting the signal along said feedback path.

37 (New). The method of claim 36 including preventing the generation of said pulse unless a pair of transistors both conduct.

38 (New). The method of claim 37 including using a capacitor circuit to enable the supply voltage to reach a designated output level.

39 (New). The method of claim 38 including coupling a hysteresis sense stage to said capacitor circuit.

40 (New). A method comprising:

using an activation circuit to determine whether a supply voltage reaches a predetermined level;

generating pulses to indicate that a supply voltage is ramping up and to terminate the generation of pulses after the supply voltage reaches a predetermined level; and

providing an inverted output of said pulse generator to said activation circuit.

41 (New). The method of claim 40 including only generating a pulse when a pair of transistors both conduct.

42 (New). The method of claim 41 including using a capacitor circuit to enable the supply voltage to reach a designated output level.

43 (New). The method of claim 42 including using a hysteresis sense stage coupled to said capacitor circuit.

REMARKS

The objection to the specification is respectfully contraverted. Claim 15 calls for an inverter that creates a high signal in response to a low signal on said feedback path. For example, referring to Figure 2, an inverter is shown connecting the RS latch 14a to the flip-flop array F, along the line 20. With respect to the requirement that a pair of transistors conduct, this